REMARKS

Claims 1-12, 13, 15, 16 and 18-23 are pending in this application. Claims 1-13, 15 and 18-21 stand allowed. Claim 16 has been amended by incorporating the subject matter of claim 17. Claim 17 has been cancelled. Claim 22 has been amended to adjust claim dependency. Because amendment of claim 16 merely incorporates subject matter of cancelled claim 17 (in compliance with 37 CFR 1.116), no new issue has been created and consideration would require only a cursory review by the Examiner. Entry of these claim amendments is respectfully solicited. This application is deemed to be in allowable condition, for the reasons set forth below.

In response to the Amendment filed on October 3, 2003, the Examiner has rejected claims 16-17 and 22-23 under 35 U.S.C. § 103(a) as being upatentable over Kuwano et al. (U.S. Patent No. 6,571,311), previously cited, in view of newly-cited Wong (U.S. Patent No. 6,160,739). The rejection is respectfully traversed.

The Examiner maintains the same position as in the previous Office Action as regards Kuwano, but holds that Kuwano in view of Wong teaches previously-added claim language "writing said second data in said second register to said memory cell to which said first data has already been written." The Examiner alleges that the combination would have been obvious "for the advantage of reducing the frequency of erase operations and to increase the endurance of non-volatile memories in order to prevent performance degradation and extend the usable lifetime of the memory." Below describes how, if the combination was properly made, the combination would fail to teach each and every element of claim 16.

Kuwano discloses an EEPROM having a simplified circuit structure accomplished by eliminating complex built-in sequencer circuits. The Examiner proposes to further enhance Kuwano by erasing data from memory cells only when the data to be stored differs from data

already stored in the memory cell, as Wong teaches. Specifically, in Wong, only those memory cells transitioning from "0" to "1" are erased. Consequently, only those memory cells transitioning from "1" to "0" are programmed. Referring to Fig. 3 of Wong, memory data currently stored is loaded into registers 320 and data to be programmed is loaded into register 330 from data input DIN. Based on a NOR operation (NOR gate 310), it is determined whether an erase operation is necessary. As a result, Wong claims to improve endurance and extend useful life of memory cells by limiting the frequency of an erase operation, on which the Examiner bases motivation. (*See* Wong, col. 4, lines 41-58).

In order to modify Kwong in the suggested manner, a word driver on the EEPROM block 114 would need to be modified in accordance with that (word line driver of Fig. 3 and element 120 of Fig. 1) of Wong for comparing data currently stored in the memory cell with data received from the EEPROM register block 102 via input DIN. Adopting the combination, the claimed first and second registers would have to be located in the EEPROM register block 102 and would not correspond to word driver registers 320, 330 of Wong. In other words, consider Fig. 4 of Kuwano which illustrates EEPROM Data Register Block 303, which is said to have a plurality of registers. The Examiner correlates these registers with the first and second data registers of claim 16. It has been further alleged that data received by these registers are from outside the memory device, as claim 16 requires. By implementing the combination, these registers would have to store memory data currently stored in the memory device and data to be programmed, as Wong teaches. (*Emphasis Added*). This would be the only way to limit the frequency of an erase operation, on which motivation is based. Because first or second register must receive data from a memory cell, claim 16 is distinguished in that the first data and the second data are each received by respective registers "from the outside of said non-volatile semiconductor memory device."

It is noted further that the principal operation of Kuwano would be rendered inoperable. The principal operation of EEPROM Data Register Block 303 is to supply data to EEPROM memory. By modifying the EEPROM Block 303 to receive data from the memory cell to limit the frequency of an erase operation, this principal operation would be rendered inoperable.

In order to expedite prosecution, claim 16 has been amended by incorporating the subject matter of claim 17 and recites "wherein said step of writing said first data overlaps with said step of storing said second data."

As regards claim 17, the Examiner alleges that Wong teaches overlapping steps at col. 10, lines 17-43. We disagree. Because data in registers 320 and 330 are used for comparison, data writing from one register would not overlap with storing data in the second register, as claim 17 would require. Specifically, Wong provides that memory cell data is sequentially loaded into associated data registers 320, and input data DIN is sequentially loaded into input registers 330. There is no disclosure that writing data to a memory cell overlaps with storing data in a register.

As distinguished above, claim 16 recited storing data "from outside the memory device," whereas the combination would require storing data from the memory cell.

As argued in previous response(s), Kuwano fails to disclose the step of writing the first data that overlaps with the step of storing the second data in the second register. By contrast, in Kuwano data is to be written to the memory cells or input to the registers only when the RA is "3H" (see Table 1 in column 8 and Fig. 5 in Kuwano). Data input to the registers during other timing are only related to control of the EEPROM in the Kuwano reference. Therefore, in Kuwano, the step of writing the first data does not overlap the step of storing the second data, as claim 16 would otherwise require.

For the foregoing reasons, claims 16, 22, and 23 are deemed distinguishable over the prior art of record, and therefore patentable. A *prima facie* case for obviousness has not been made, thus rendering the rejection improper. Withdrawal of the rejection is respectfully solicited.

If the Examiner has any comments or questions regarding this response or the application in general, the Examiner is encouraged to contact the undersigned in order to expedite prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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